LC²MOS Octal 8-Bit DAC

Data Sheet

AD7228

FEATURES

- Eight 8-bit DACs with output amplifiers
- Operates with single or dual supplies
- Microprocessor-compatible (95 ns $\overline{WR}$ pulse)
- No user trims required
- Skinny 24-lead PDIP, CERDIP, and SOIC packages, and a 28-lead PLCC surface-mount package

FUNCTIONAL BLOCK DIAGRAM

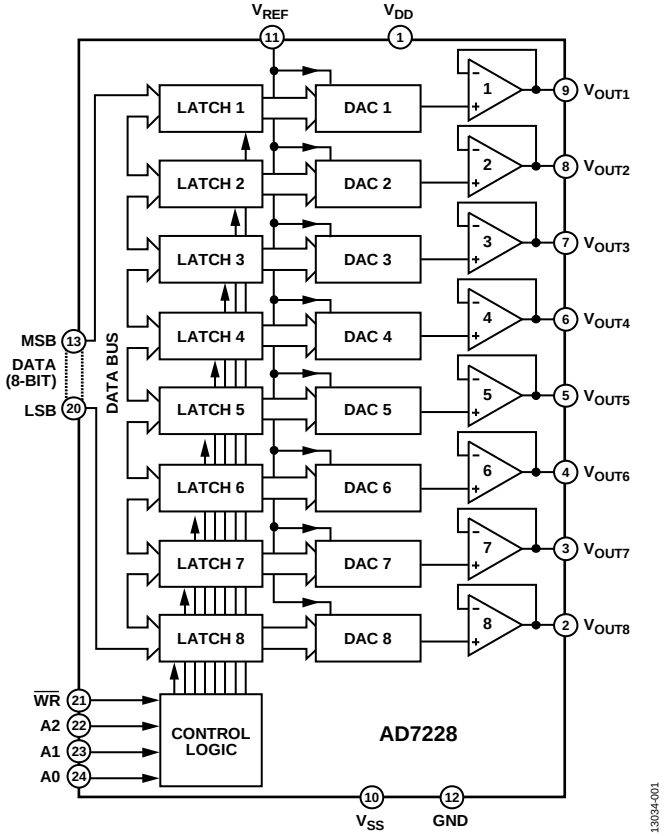

Figure 1.

GENERAL DESCRIPTION

The AD7228 contains eight 8-bit voltage mode digital-to- analog converters (DACs), with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve the full specified performance for the device.

Separate on-chip latches are provided for each of the eight DACs. Data is transferred into the data latches through a common 8-bit, TTL/CMOS-compatible input port (5 V). The A0, A1, and A2 address inputs determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from 2 V to 10 V when using dual supplies. The device is also specified for single-supply operation using a reference of 10 V. Each output buffer amplifier is capable of developing 10 V across a 2 kΩ load.

The AD7228 is fabricated on an all ion implanted, high speed, linear-compatible CMOS (LC²MOS) process, specifically developed to integrate high speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. The single chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. The PDIP, CERDIP, and SOIC pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. The voltage mode configuration of the DACs allows single supply operation of the AD7228. The device can also be operated with dual supplies giving enhanced performance for some parameters.
3. The AD7228 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high performance 8-bit microprocessors.

Rev. D

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AD7228* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD7228: Military Data Sheet
- AD7228: LC2MOS Octal 8-Bit DAC Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD7228 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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TABLE OF CONTENTS

REVISION HISTORY

10/2017—Rev. C to Rev. D

Changes to Ordering Guide ... 15

12/2015—Rev. B to Rev. C

Changes to Features Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Deleted LCCC Pin Configuration ... 4
Changes to Table 3 ... 5
Changes to Absolute Maximum Ratings Section and Table 4 ... 6
Added Table 5; Renumbered Sequentially ... 7
Added 5 V Single-Supply Operation Section ... 12
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 10.8 V to 16.5 V, V_{SS} = −5 V ± 10%, GND = 0 V, V_{REF} = 2 V to 10 V, R_L = 2 kΩ, C_L = 100 pF, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, −40°C to +85°C unless otherwise noted. V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.

Table 1.

Parameter	K and B Versions	L and C Versions	Unit	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error (TUE)[1]	±2	±1	LSB max	V_{DD} = 15 V ± 10%, V_{REF} = 10 V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed monotonic
Full-Scale Error[2]	±1	±1/2	LSB max	Typical temperature coefficient is 5 ppm/°C with V_{REF} = 10 V
Zero Code Error				
at 25°C	±25	±15	mV max	Typical temperature coefficient is 30 µV/°C
T_{MIN} to T_{MAX}	±30	±20	mV max	
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = 10 V
REFERENCE INPUT				
Voltage Range	2/10	2/10	V min/V max	
Input Resistance	2	2	kΩ min	
Input Capacitance[3]	500	500	pF max	Occurs when each DAC is loaded with all 1s
AC Feedthrough	−70	−70	dB typ	V_{REF} = 8 V p-p sine wave at 10 kHz
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE[3]				
Voltage Output Slew Rate	2	2	V/µs min	
Voltage Output Settling Time				
Positive Full-Scale Change	5	5	µs max	V_{REF} = 10 V; settling time to ±1/2 LSB
Negative Full-Scale Change	5	5	µs max	V_{REF} = 10 V; settling time to ±1/2 LSB
Digital Feedthrough	50	50	nV-sec typ	Code transition all 0s to all 1s, V_{REF} = 0 V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[4]	50	50	nV-sec typ	Code transition all 0s to all 1s, V_{REF} = 10 V; $\overline{WR}$ = 0 V
POWER SUPPLIES				
V_{DD} Range	10.8/16.5	10.8/16.5	V min/V max	For specified performance
V_{SS} Range	−4.5/−5.5	−4.5/−5.5	V min/V max	For specified performance
I_{DD}				Outputs unloaded; V_{IN} = V_{INL} or V_{INH}
at 25°C	16	16	mA max	
T_{MIN} to T_{MAX}	20	20	mA max	
I_{SS}				Outputs unloaded; V_{IN} = V_{INL} or V_{INH}
at 25°C	14	14	mA max	
T_{MIN} to T_{MAX}	18	18	mA max	

[1] Total unadjusted error includes zero code error, relative accuracy, and full-scale error.
[2] Calculated after zero code error is adjusted out.
[3] Sample tested at T_A = 25°C to ensure compliance.
[4] The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.

SINGLE SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = GND, GND = 0 V, V_{REF} = 10 V, R_L = 2 kΩ, C_L = 100 pF, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	K and B Versions	L and C Versions	Unit	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error[1]	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed monotonic
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = 10 V
REFERENCE INPUT				
Input Resistance	2	2	kΩ min	
Input Capacitance[2]	500	500	pF max	Occurs when each DAC is loaded with all 1s
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[2]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE[2]				
Voltage Output Slew Rate	2	2	V/µs min	
Voltage Output Settling Time				
Positive Full-Scale Change	5	5	µs max	Settling time to ±1/2 LSB
Negative Full-Scale Change	7	7	µs max	Settling time to ±1/2 LSB
Digital Feedthrough	50	50	nV-sec typ	Code transition all 0s to all 1s, V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[3]	50	50	nV-sec typ	Code transition all 0s to all 1s, V_{REF} = 10 V, $\overline{WR}$ = 0 V
POWER SUPPLIES				
V_{DD} Range	13.5/16.5	13.5/16.5	V min/V max	For specified performance
I_{DD}				Outputs unloaded; V_{IN} = V_{INL} or V_{INH}
at 25°C	16	16	mA max	
T_{MIN} to T_{MAX}	20	20	mA max	

[1] Total unadjusted error includes zero code error, relative accuracy and full-scale error.
[2] Sample tested at T_A = 25°C to ensure compliance.
[3] The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.

SWITCHING CHARACTERISTICS

See Figure 8 and Figure 2; V_{DD} = 5 V ± 5% or 10.8 V to 16.5 V; V_{SS} = 0 V or –5 V ± 10%. Sample tested at 25°C to ensure compliance. All input rise and fall times measured from 10% to 90% of 5 V, $t_R = t_F$ = 5 ns. Timing measurement reference level is $(V_{INH} + V_{INL})/2$.

Table 3.

Parameter	Limit at 25°C, All Grades	Limit at T_{MIN}, T_{MAX}, K, L, B, and C Versions	Unit	Description
t_1	0	0	ns min	Address to $\overline{WR}$ setup time
t_2	0	0	ns min	Address to $\overline{WR}$ hold time
t_3	70	90	ns min	Data valid to $\overline{WR}$ setup time
t_4	10	10	ns min	Data valid to $\overline{WR}$ hold time
t_5	95	120	ns min	Write pulse width

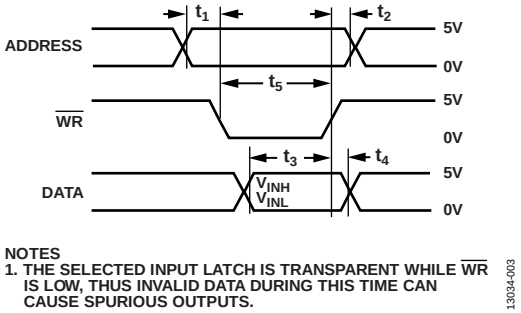


Figure 2. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +17 V
V_{DD} to V_{SS}	−0.3 V to +24 V
Digital Input Voltage to GND	−0.3 V to V_{DD}
V_{REF} to GND	−0.3 V to V_{DD}
V_{OUTx} to GND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to 75°C	1000 mW
Derates Above 75°C by	2.0 mW/°C
Operating Temperature Range	
Commercial	−40°C to +85°C
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Outputs can be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short-circuit current fora short to GND or V_{SS} is 50 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

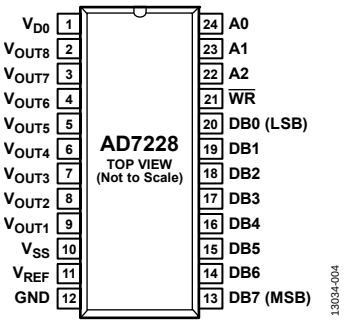


Figure 3. 24-Lead PDIP, CERDIP, and SOIC Pin Configuration

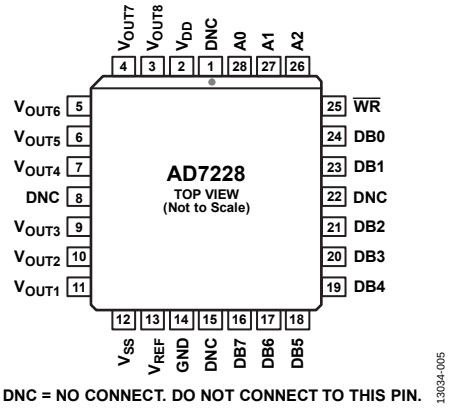


Figure 4. 28-Lead PLCC Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
24-Lead PDIP, CERDIP, and SOIC	**28-Lead PLCC**	**Mnemonic**	**Description**
1	2	V_{DD}	Positive Supply Voltage This device can be operated from a supply of 10.8 V to 16.5 V.
2	3	V_{OUT8}	Analog Output Voltage of DAC 8.
3	4	V_{OUT7}	Analog Output Voltage of DAC 7.
4	5	V_{OUT6}	Analog Output Voltage of DAC 6.
5	6	V_{OUT5}	Analog Output Voltage of DAC 5.
6	7	V_{OUT4}	Analog Output Voltage of DAC 4.
	1, 8, 15, 22	DNC	Do Not Connect. Do not connect to this pin.
7	9	V_{OUT3}	Analog Output Voltage of DAC 3.
8	10	V_{OUT2}	Analog Output Voltage of DAC 2.
9	11	V_{OUT1}	Analog Output Voltage of DAC 1.
10	12	V_{SS}	Negative Supply Voltage. This device can be operated from a supply of −5.5 V to −4.5 V.
11	13	V_{REF}	DAC Reference Voltage Input.
12	14	GND	Ground Pin.
13	16	DB7	Parallel Data Bit 7.
14	17	DB6	Parallel Data Bit 6.
15	18	DB5	Parallel Data Bit 5.
16	19	DB4	Parallel Data Bit 4.
17	20	DB3	Parallel Data Bit 3.
18	21	DB2	Parallel Data Bit 2.
19	23	DB1	Parallel Data Bit 1.
20	24	DB0	Parallel Data Bit 0.
21	25	$\overline{WR}$	Write Control Digital Input In, Active Low. $\overline{WR}$ transfers shift register data to the DAC register on the rising edge. The signal level on this pin must be ≤ V_{DD} + 0.3 V.
22	26	A2	Address Pin 2. The signal level on this pin must be ≤ V_{DD} + 0.3 V.
23	27	A1	Address Pin 1. The signal level on this pin must be ≤ V_{DD} + 0.3 V.
24	28	A0	Address Pin 0. The signal level on this pin must be ≤ V_{DD} + 0.3 V.

THEORY OF OPERATION

CIRCUIT INFORMATION

DACs

The AD7228 contains eight identical, 8-bit, voltage mode DACs. The output voltages from the converters have the same polarity as the reference voltage, allowing single-supply operation. A novel DAC switch pair arrangement on the AD7228 allows a reference voltage range from 2 V to 10 V. Each DAC consists of a highly stable, thin film, R-2R ladder and eight high speed NMOS switches. The simplified circuit diagram for one channel is shown in Figure 5. Note that V_{REF} and GND are common to all eight DACs.

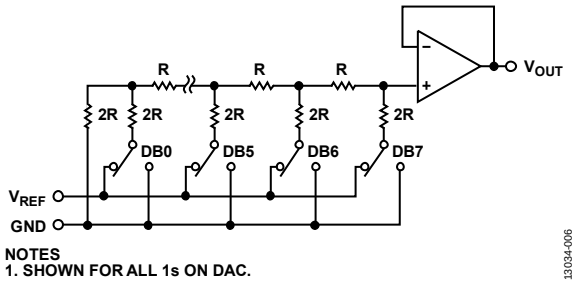


Figure 5. DAC Simplified Circuit Diagram

The input impedance at the V_{REF} pin of the AD7228 is the parallel combination of the eight individual DAC reference input impedances. It is code dependent and can vary from 2 kΩ to infinity. The lowest input impedance occurs when all eight DACs are loaded with digital code 01010101. Therefore, it is important that the external reference source presents a low output impedance to the V_{REF} terminal of the AD7228 under changing load conditions. Due to transient currents at the reference input during digital code changes, a 0.1 µF (or greater) decoupling capacitor is recommended on the V_{REF} input for dc applications. The nodal capacitance at the reference terminal is also code dependent and typically varies from 120 pF to 350 pF.

Consider each V_{OUTX} pin as a digitally programmable voltage source with an output voltage.

$$V_{OUTx} = D_N \times V_{REF}$$

where D_N is a fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier as described in the Op Amp section.

Op Amp

Each voltage mode DAC output is buffered by a unity-gain, noninverting, CMOS amplifier. This buffer amplifier is tested with a 2 kΩ and 100 pF load, but typically drives a 2 kΩ and 500 pF load.

The AD7228 can be operated from single or dual supplies. Operating the device from single or dual supplies has no effect on the positive going settling time. However, the negative going settling time to voltages near 0 V in single-supply operation is slightly longer than the settling time for dual supply operation. Additionally, to ensure that the output voltage can go to 0 V in single-supply operation, a transistor on the output acts as a passive pull-down as the output voltage nears 0 V. As a result, the sink capability of the amplifier is reduced as the output voltage nears 0 V in single-supply operation. In dual supply operation, the full sink capability of 400 µA at 25°C is maintained over the entire output voltage range. The single-supply output sink capability is shown in Figure 6. The negative V_{SS} also gives improved output amplifier performance, allowing an extended input reference voltage range and giving an improved slew rate at the output.

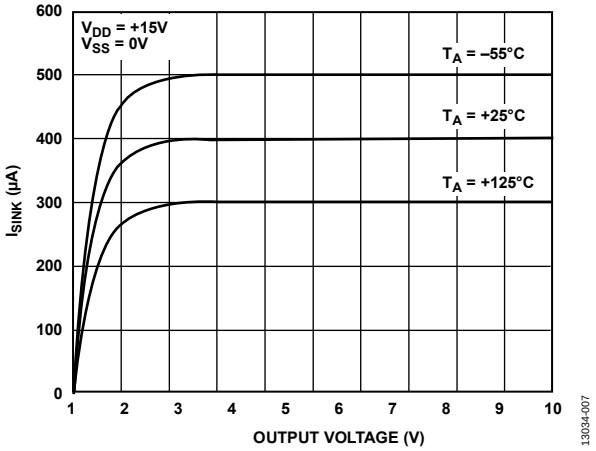


Figure 6. Single Supply Sink Current

The output broadband noise from the amplifier is 300 µV p-p. Figure 7 shows a plot of noise spectral density vs. frequency.

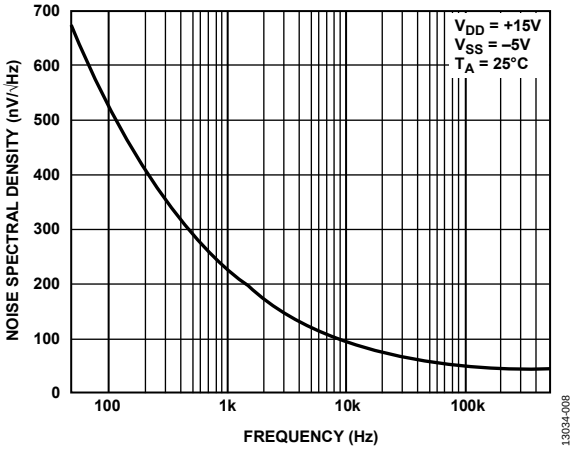


Figure 7. Noise Spectral Density vs. Frequency

Digital Inputs

The AD7228 digital inputs are compatible with either TTL or 5 V CMOS levels. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA. Internal input protection is achieved by on-chip distributed diodes.

Interface Logic Information

The A0, A1, and A2 address lines select which DAC accepts data from the input port. Table 6 shows the selection table for the eight DACs and Figure 8 shows the input control logic. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

Table 6. AD7228 Truth Table

Control Inputs				
$\overline{WR}$	A2	A1	A0	Operation
High	X[1]	X	X	No operation, device not selected
Low	Low	Low	Low	DAC 1 transparent
Low to High	Low	Low	Low	DAC 1 latched
Low	Low	Low	High	DAC 2 transparent
Low	Low	High	Low	DAC 3 transparent
Low	Low	High	High	DAC 4 transparent
Low	High	Low	Low	DAC 5 transparent
Low	High	Low	High	DAC 6 transparent
Low	High	High	Low	DAC 7 transparent
Low	High	High	High	DAC 8 transparent

[1] X means don't care.

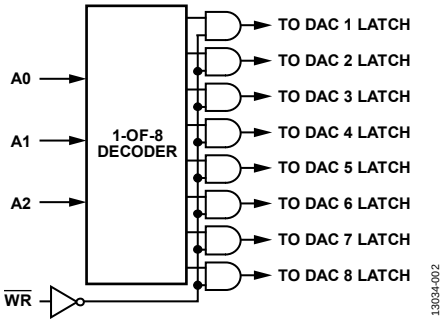


Figure 8. Input Control Logic

Supply Current

The AD7228 has a maximum I_{DD} specification of 20 mA and a maximum I_{SS} of 18 mA over the −40°C to +85°C temperature range. Figure 9 shows a typical plot of power supply current vs. temperature.

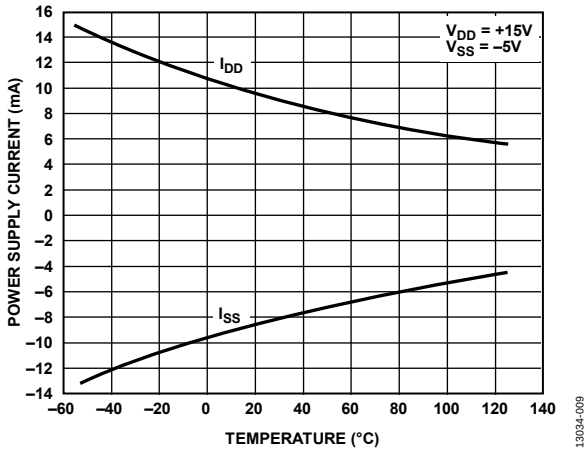


Figure 9. Power Supply Current vs. Temperature

Applying the AD7228 Unipolar Output Operation

Unipolar output operation is the basic mode of operation for each channel of the AD7228 and the output voltage has the same positive polarity as V_{REF}. Connections for unipolar output operation are shown in Figure 10. The AD7228 can be operated from single or dual supplies. The voltage at the reference input must never be negative with respect to GND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table 7.

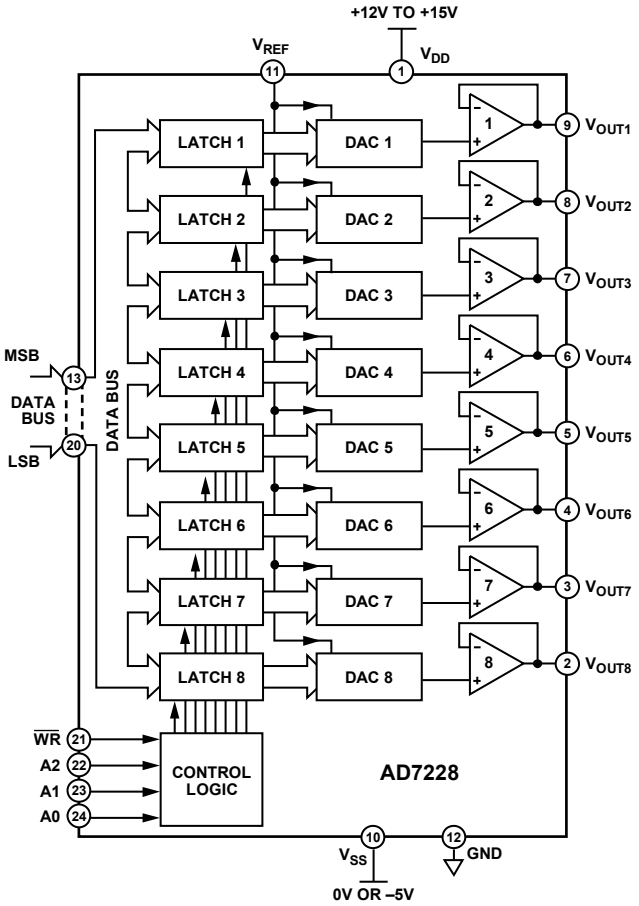


Figure 10. Unipolar Output Circuit

Table 7. Unipolar Code Table

DAC Latch Contents		
MSB	**LSB[1]**	**Analog Output**
1 1 1 1	1 1 1 1	$+V_{REF}(255/256)$
1 0 0 0	0 0 0 1	$+V_{REF}(129/256)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}(127/256)$
0 0 0 0	0 0 0 1	$+V_{REF}(1/256)$
0 0 0 0	0 0 0 0	0 V

[1] 1 LSB = $(V_{REF})(2^{-8}) = V_{REF}$ (1/256).

Bipolar Output Operation

Each of the DACs on the AD7228 can be individually configured for bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 11 shows a circuit used to implement offset binary coding (bipolar operation) with DAC 1 of the AD7228. In this case,

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \times (D_1 \times V_{REF}) - \left(\frac{R2}{R1}\right) \times (V_{REF})$$

With $R1 = R2$,

$$V_{OUT} = (2D_1 - 1) \times (V_{REF})$$

where D_1 is a fractional representation of the digital word in Latch 1 of the AD7228 ($0 \le D_1 \le 255/256$).

Table 8. Bipolar Code Table

DAC Latch Contents		
MSB	**LSB**	**Analog Output**
1 1 1 1	1 1 1 1	$+V_{REF}(127/128)$
1 0 0 0	0 0 0 1	$+V_{REF}(1/128)$
1 0 0 0	0 0 0 0	0 V
0 1 1 1	1 1 1 1	$-V_{REF}(1/128)$
0 0 0 0	0 0 0 1	$-V_{REF}(127/128)$
0 0 0 0	0 0 0 0	$-V_{REF}(128/128) = -V_{REF}$

Mismatch between R1 and R2 causes gain and offset errors; therefore, these resistors must match and track over temperature.

The AD7228 can be operated from a single supply or from dual supplies. Table 8 shows the digital code vs. output voltage relationship for the circuit of Figure 11 with R1 = R2.

AC Reference Signal

In some applications, it may be desirable to have an ac signal applied as the reference input to the AD7228. The AD7228 has multiplying capability within the upper (10 V) and lower (2 V) limits of reference voltage when operated with dual supplies. Therefore, ac signals must be ac-coupled and biased up before being applied to the reference input. Figure 12 shows an ac signal applied to the reference input of the AD7228. For input frequencies up to 50 kHz, the output distortion typically remains less than 0.1%. The typical 3 dB bandwidth for small signal inputs is 800 kHz.

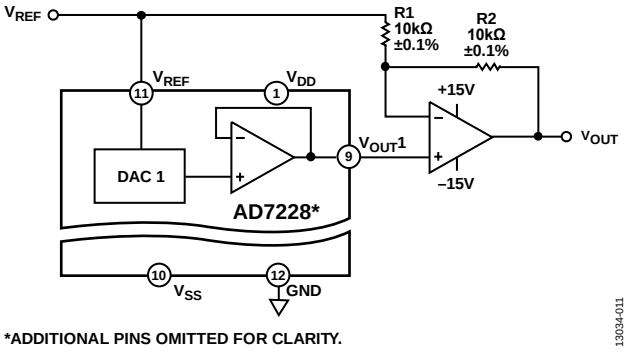


Figure 11. Bipolar Output Circuit

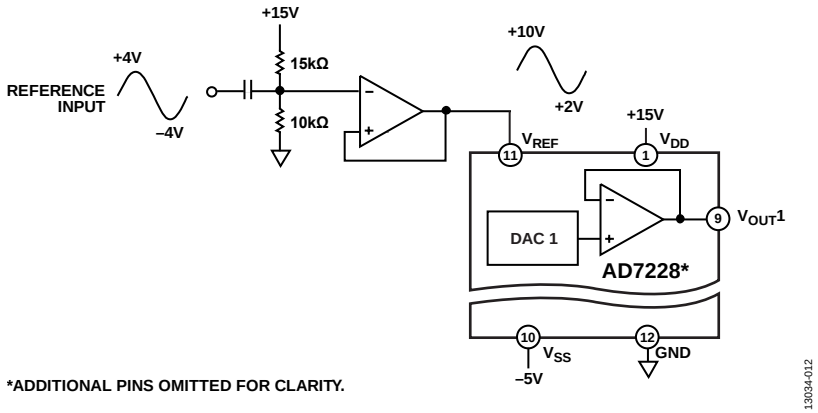


Figure 12. Applying an AC Signal to the AD7228

Timing Deskew

Signal edges slowing or rounding off by the time they reach the pin driver circuitry is a common problem in automated test equipment (ATE) applications. Square up the edge at the pin driver to overcome this problem. However, because each edge is not rounded off by the same extent, this squaring up may lead to incorrect timing relationship between signals. This effect is shown in Figure 13.

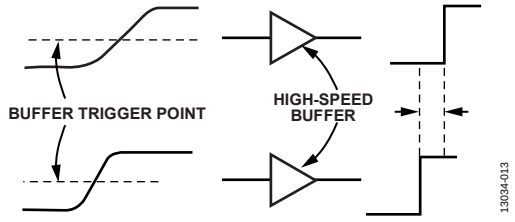


Figure 13. Time Skewing Due to Slowing of Edges

The circuit of Figure 14 shows how two DACs of the AD7228 can help overcome the problem of time skewing. The same two signals are applied to this circuit as are applied in Figure 14. The output of each DAC is applied to one input of a high speed comparator, and the signals are applied to the other inputs. Varying the output voltage of the DAC effectively varies the trigger point at which the comparator flips. Therefore, the timing relationship between the two signals can be programmably corrected (or deskewed) by varying the code to the DAC of the AD7228. In a typical application, the code is loaded to the DACs for correct timing relationships during the calibration cycle of the instrument.

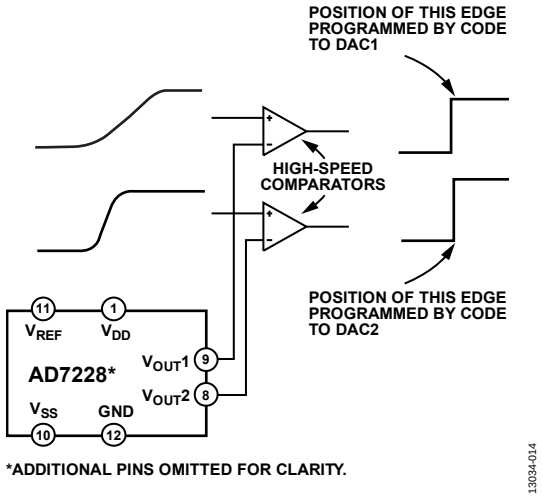


Figure 14. AD7228 Timing Deskew Circuit

Coarse/Fine Adjust

Pair the DACs on the AD7228 together to form a coarse/fine adjust function as shown in Figure 15. The function is achieved using one external op amp and a few resistors per pair of DACs.

DAC 1 is the most significant or coarse DAC. Data is first loaded to this DAC to coarsely set the output voltage. DAC 2 is then used to fine tune this output voltage. Varying the ratio of R1 to R2 varies the relative effect of the coarse and fine DACs on the output voltage. For the resistor values shown, DAC 2 has a resolution of 150 µV in a 10 V output range. Because each DAC on the AD7228 is guaranteed monotonic, the coarse adjustment and fine adjustment are each monotonic. One application for this is as a setpoint controller (see the AN-317 Application Note, "*Circuit Applications of the AD7226 Quad CMOS DAC,*" available from Analog Devices, Inc.).

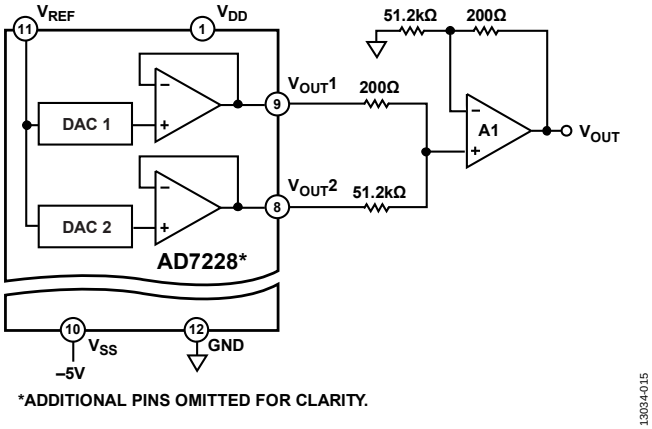


Figure 15. Coarse/Fine Adjust Circuit

Self Programmable Reference

The circuit of Figure 16 shows how one DAC of the AD7228, in this case DAC 1, can be used in a feedback configuration to provide a programmable reference for itself and the other seven converters. The relationship of V_{REF} to V_{IN} is expressed by

$$V_{REF} = \frac{(1+G)}{(1+G \times D_1)} \times V_{IN}$$

where G = R2/R1.

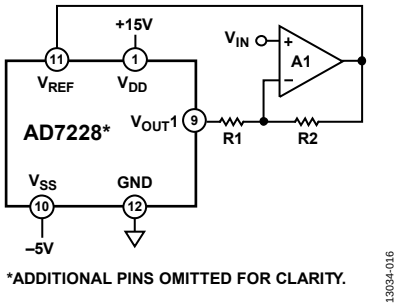


Figure 16. Self Programmable Reference

Figure 17 shows typical plots of V_{REF} vs. digital code, D_1, for three different values of G. With V_{IN} = 2.5 V and G = 3, the voltage at the output varies between 2.5 V and 10 V, giving an effective 10-bit dynamic range to the other seven converters. For correct operation of the circuit, it is recommended that V_{SS} is equal to −5 V and R1 be greater than 6.8 kΩ.

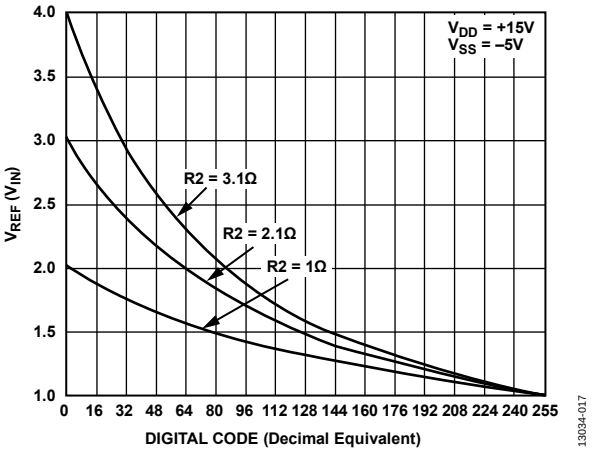


Figure 17. Variation of V_{REF} with Feedback Configuration

5 V Single-Supply Operation

The AD7228 can be operated from a single 5 V power supply, resulting in only slightly degraded accuracy performance from the device. Figure 18 shows a typical plot of relative accuracy for the device with V_{DD} = 5 V and a reference voltage of 1.23 V. Differential nonlinearity is an important parameter that retains its specified performance and remains monotonic over the output voltage range.

The output transfer function sits on top of the amplifier offset voltage; there is an initial offset voltage, and the voltage coming from the output transfer function is added on top of this offset voltage. Because the reference voltage is reduced, the offset voltage equals a few LSBs. For devices with a true negative offset (when V_{SS} = −5 V), the transfer function does not move off the bottom rail for the first few LSBs of code. After this, the transfer function continues as normal. The relative accuracy plot of Figure 18 is for a device with a true positive offset.

Maintain the required overhead voltage of 3.5 V between V_{DD} and the reference voltage, which limits the reference voltage range. However, operating the device from a single 5 V supply reduces the power dissipation considerably (typically to 50 mW). The digital input threshold levels and digital input currents are not affected by operating the device from the single 5 V supply.

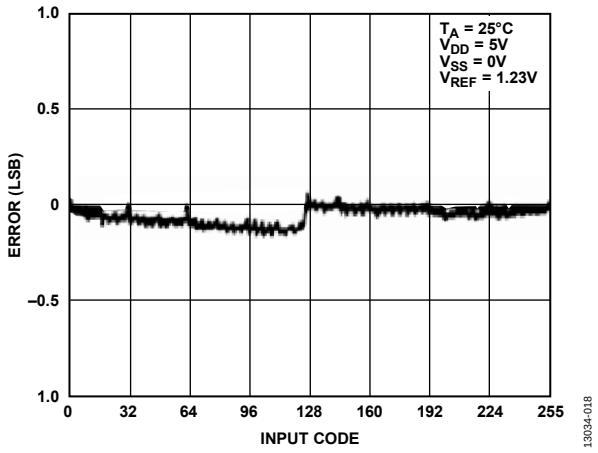


Figure 18. Relative Accuracy at V_{DD} = 5 V

Microprocessor Interfacing

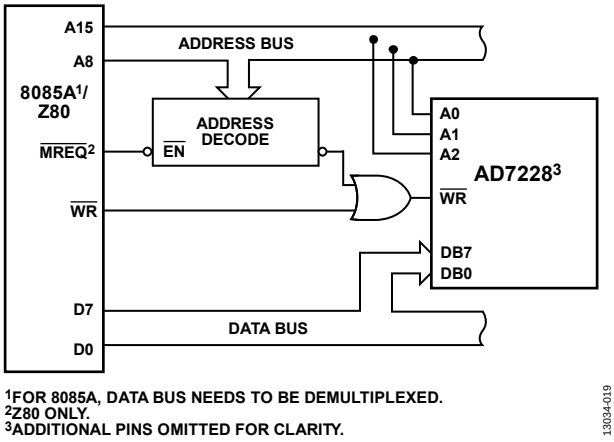


Figure 19. AD7228 to 8085A/Z80 Interface

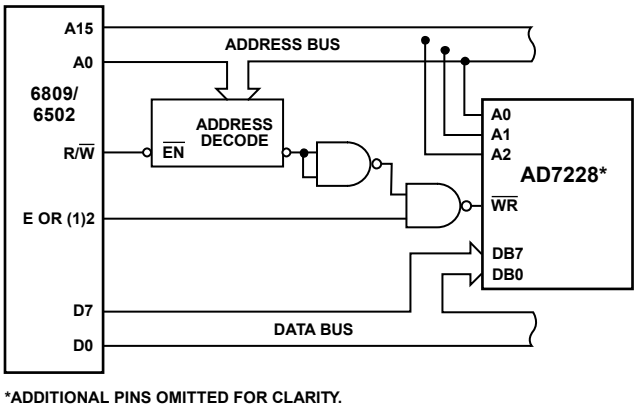
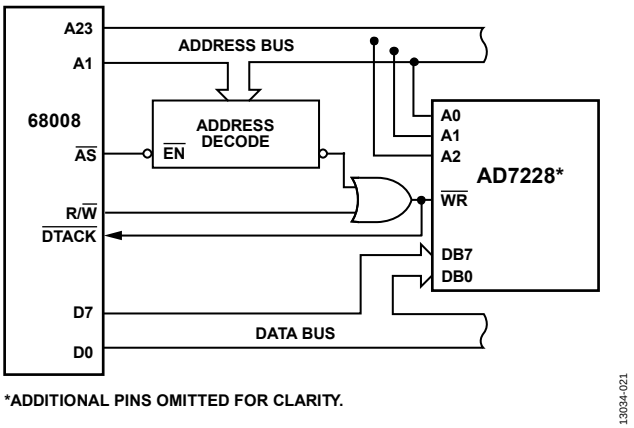
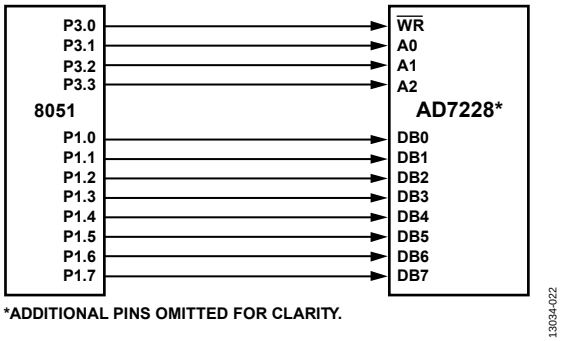


Figure 20. AD7228 to 6809/6502 Interface



*ADDITIONAL PINS OMITTED FOR CLARITY.

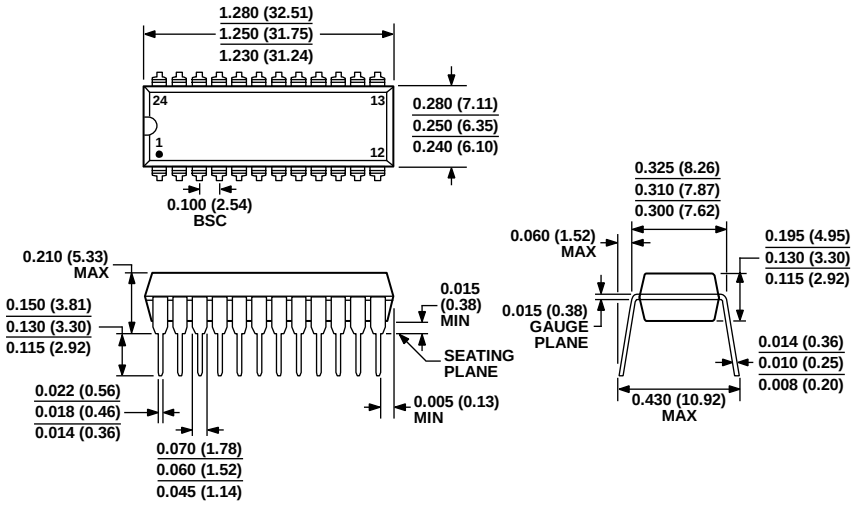
Figure 21. AD7228 to 68008 Interface



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 22. AD7228 to 8051 Interface

OUTLINE DIMENSIONS

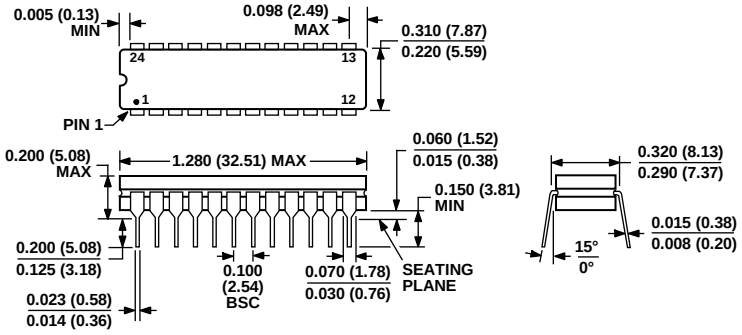


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

071006-A

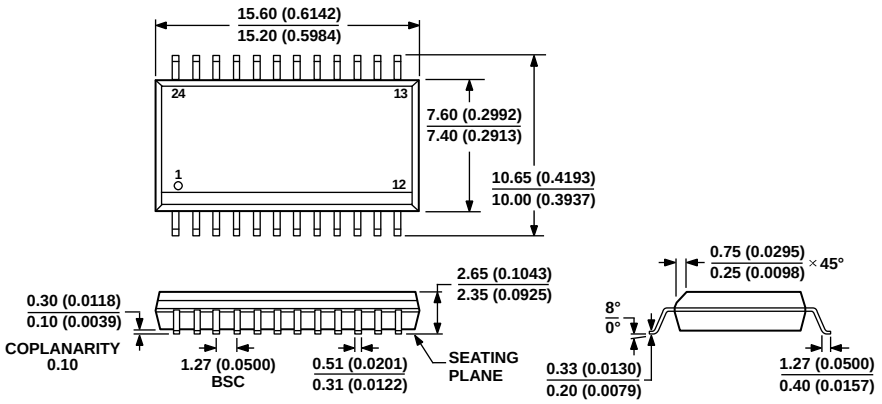
Figure 23. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-24-1)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

100808-A

Figure 24. 24-Lead Ceramic Dual In-Line Package [CERDIP]
Narrow Body (Q-24-1)
Dimensions shown in inches and (millimeters)



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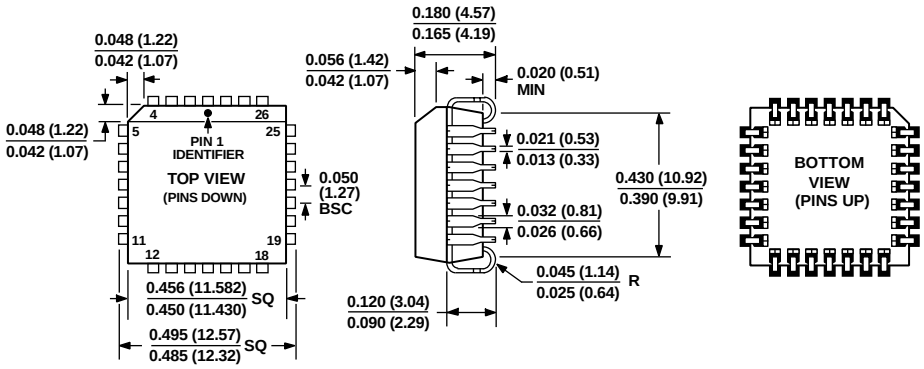
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

12-09-2010-A

Figure 25. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-24)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-047-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

042508-A

Figure 26. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Maximum TUE (LSB)	Package Description	Package Option
AD7228BQ	−40°C to +85°C	±2	24-Lead CERDIP	Q-24-1
AD7228CQ	−40°C to +85°C	±1	24-Lead CERDIP	Q-24-1
AD7228KN	−40°C to +85°C	±2	24-Lead PDIP	N-24-1
AD7228KNZ	−40°C to +85°C	±2	24-Lead PDIP	N-24-1
AD7228KP	−40°C to +85°C	±2	28-Lead PLCC	P-28
AD7228KP-REEL	−40°C to +85°C	±2	28-Lead PLCC	P-28
AD7228KPZ	−40°C to +85°C	±2	28-Lead PLCC	P-28
AD7228KR	−40°C to +85°C	±2	24-Lead SOIC_W	RW-24
AD7228KRZ	−40°C to +85°C	±2	24-Lead SOIC_W	RW-24
AD7228LNZ	−40°C to +85°C	±1	24-Lead PDIP	N-24-1
AD7228LPZ	−40°C to +85°C	±1	28-Lead PLCC	P-28

[1] Z = RoHS Compliant Part.